

FIGURE 1A
(PRIOR ART)

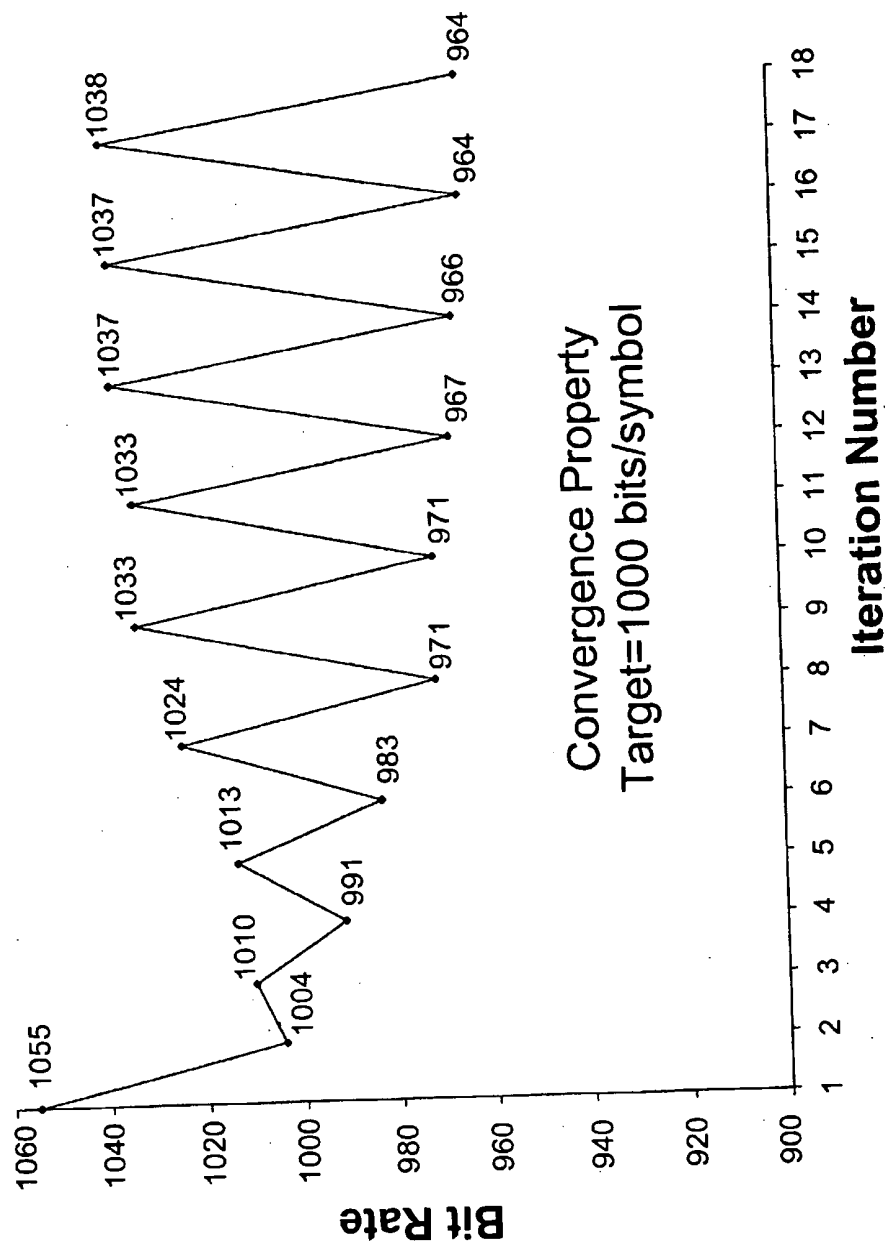
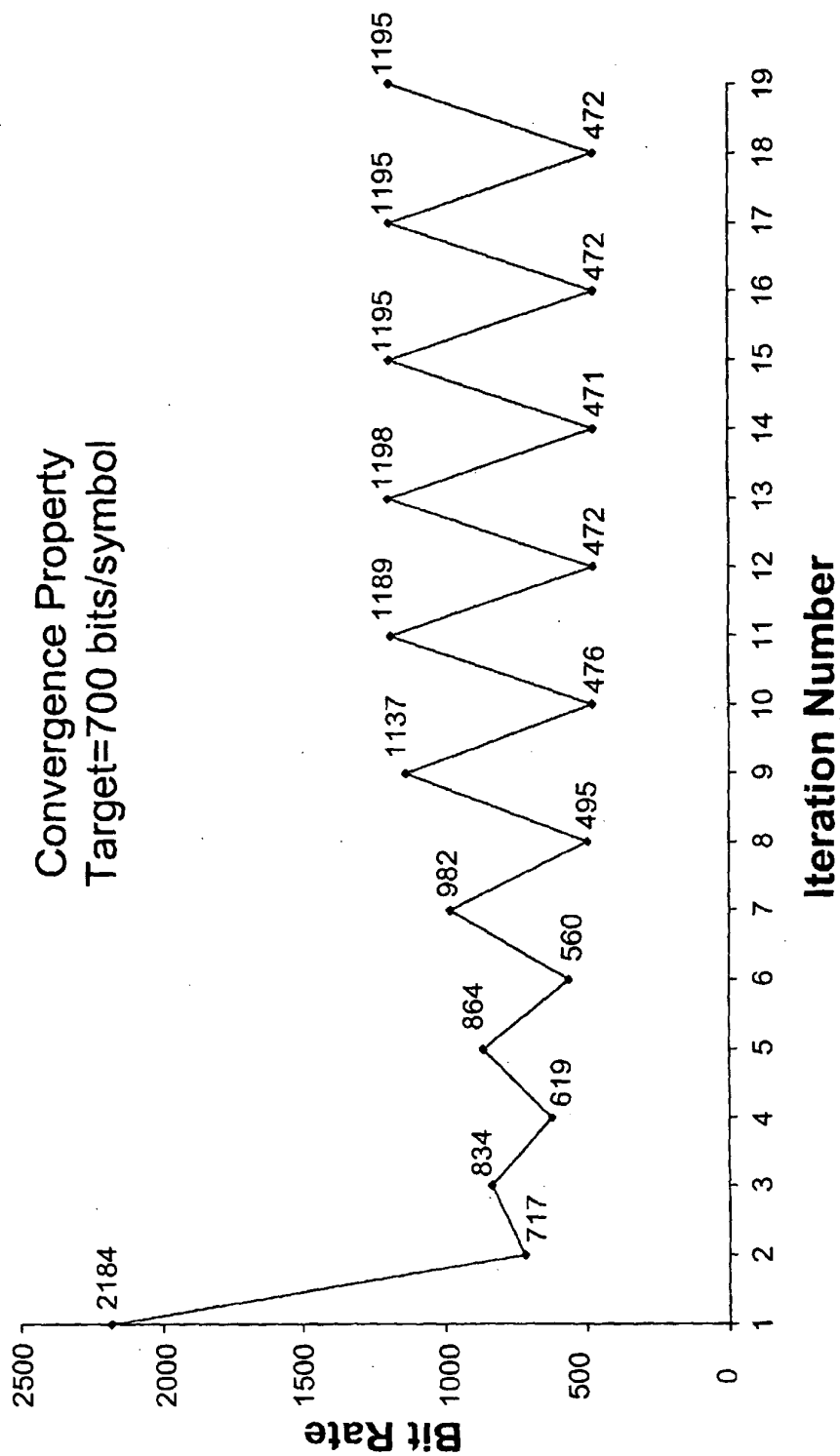


FIGURE 1B
(PRIOR ART)

Convergence Property
Target=700 bits/symbol



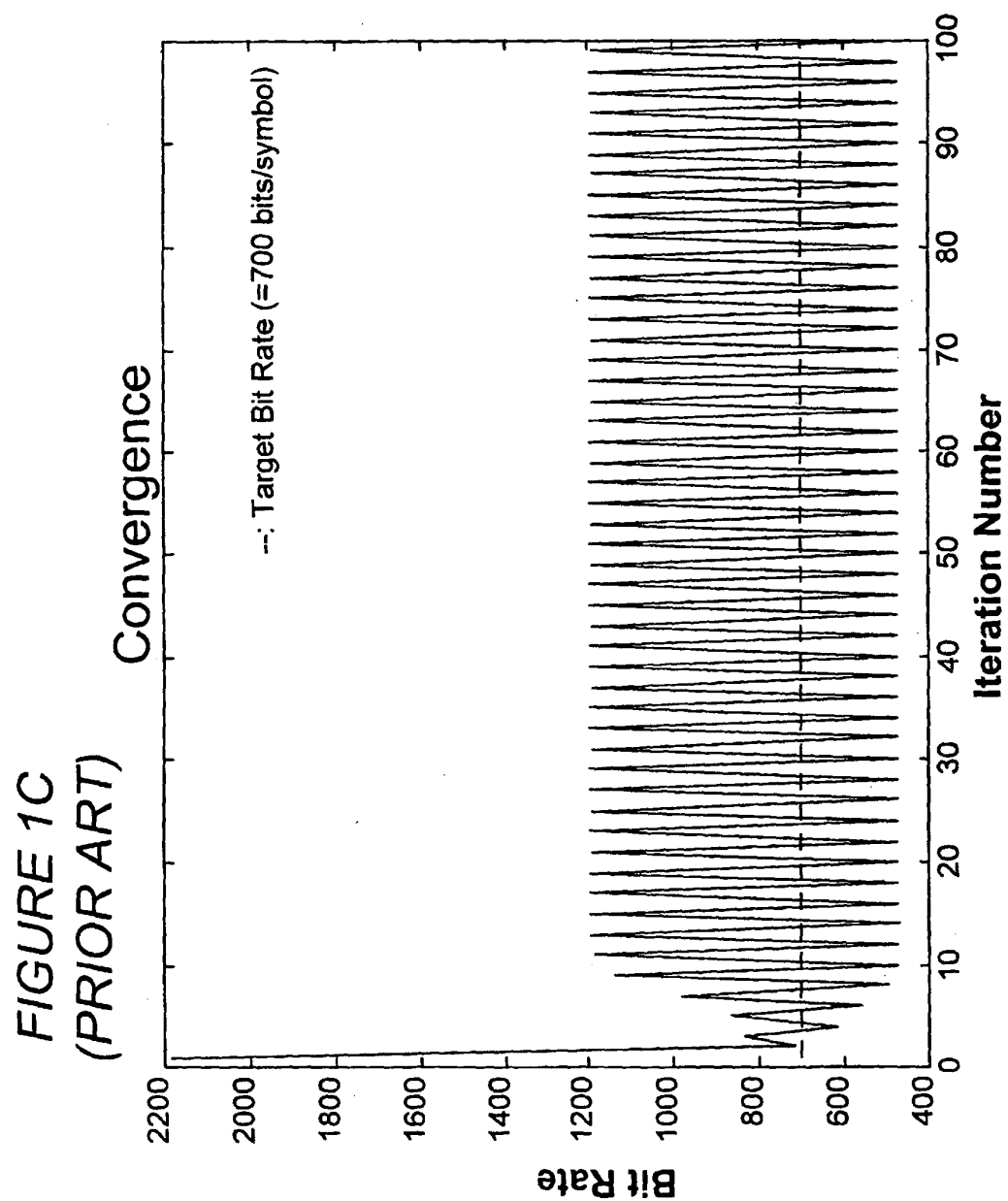


FIGURE 2
(Prior Art)

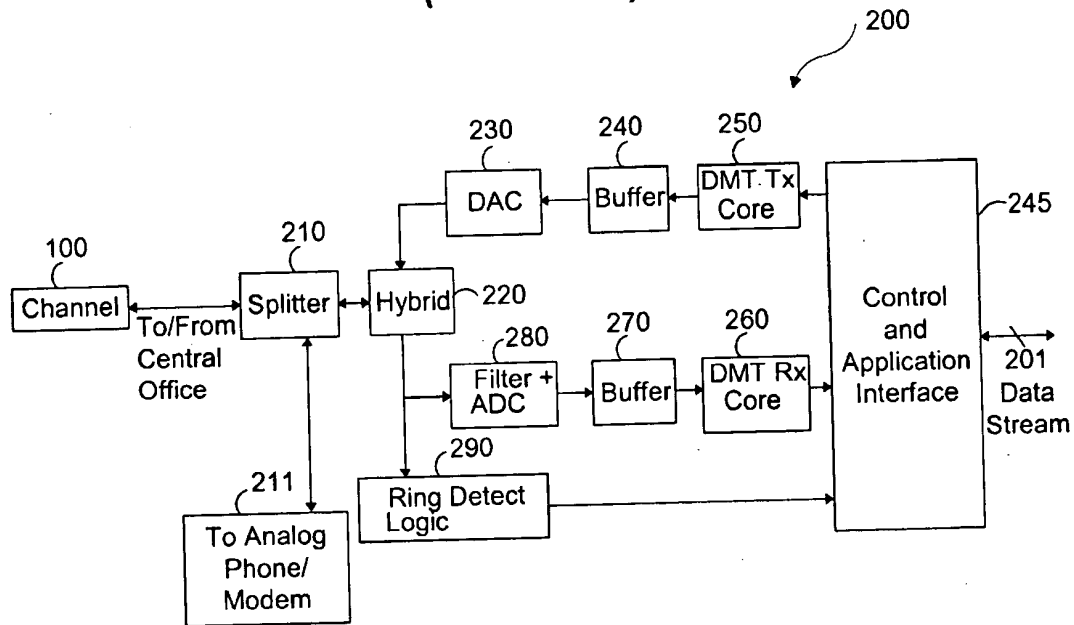


FIGURE 3

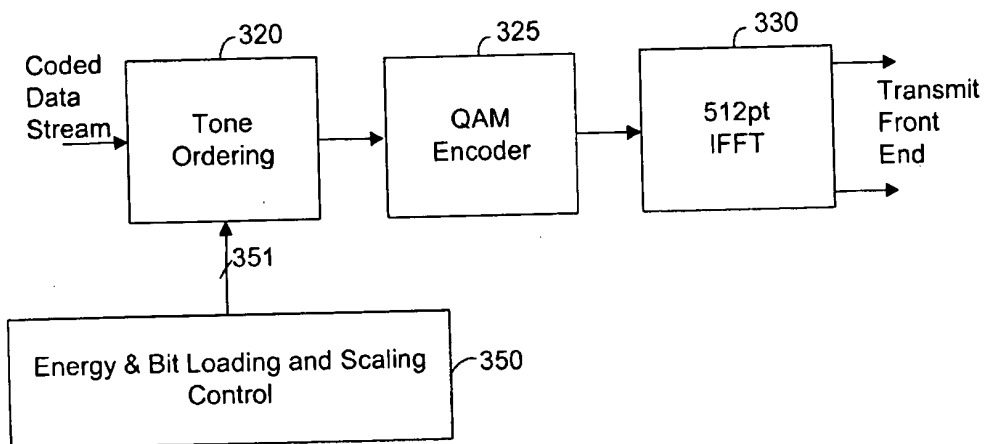


FIGURE 4

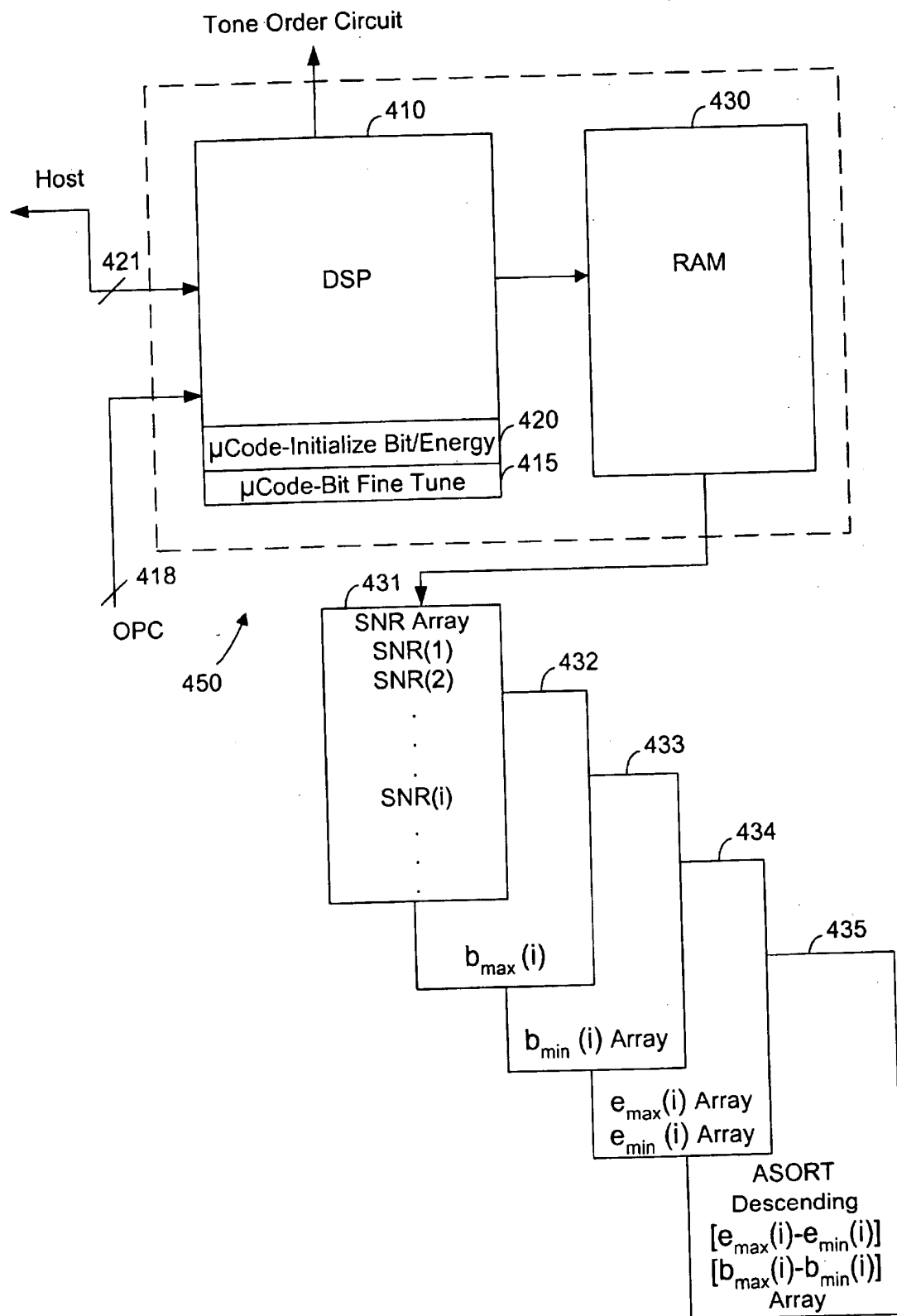


FIGURE 5

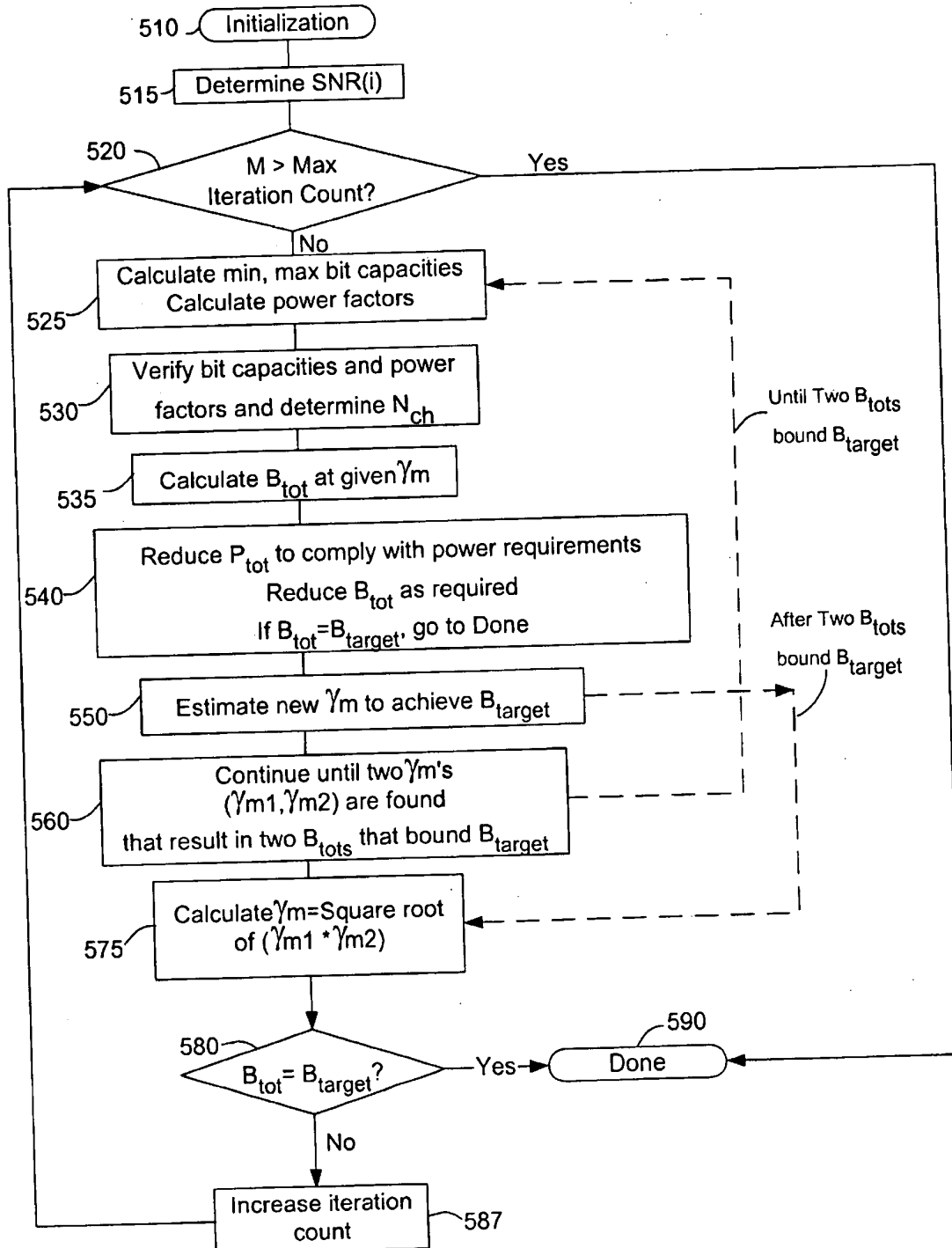
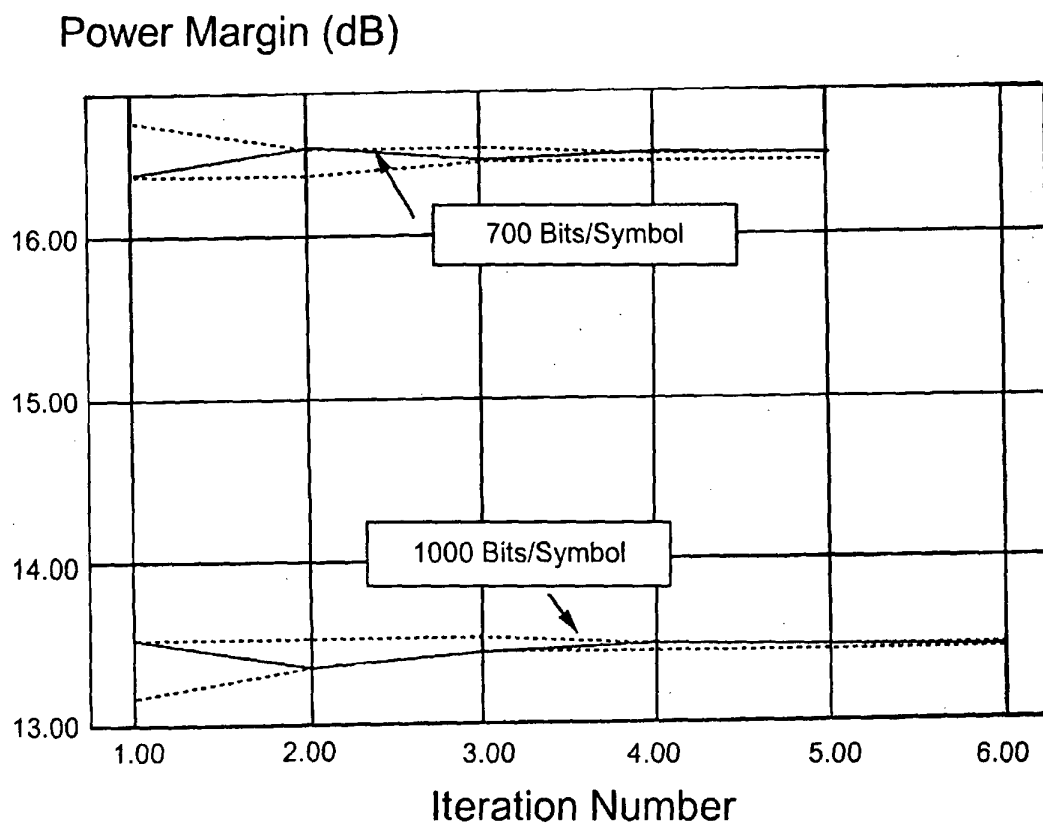


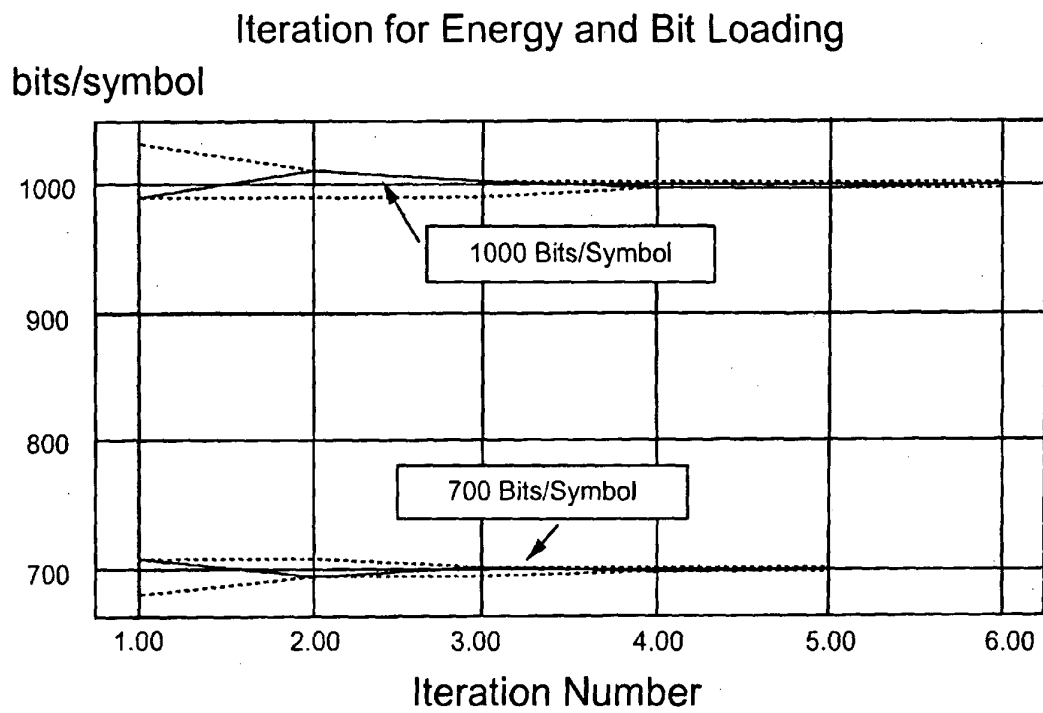
FIGURE 6A

Iteration for Energy Bit Loading



Solid Lines: power margin during iteration

Dotted Lines: interval limits during binary iteration

FIGURE 6B

Solid Lines: power margin during iteration

Dotted Lines: interval limits during binary iteration

FIGURE 7

Bit Fine Tune Procedure

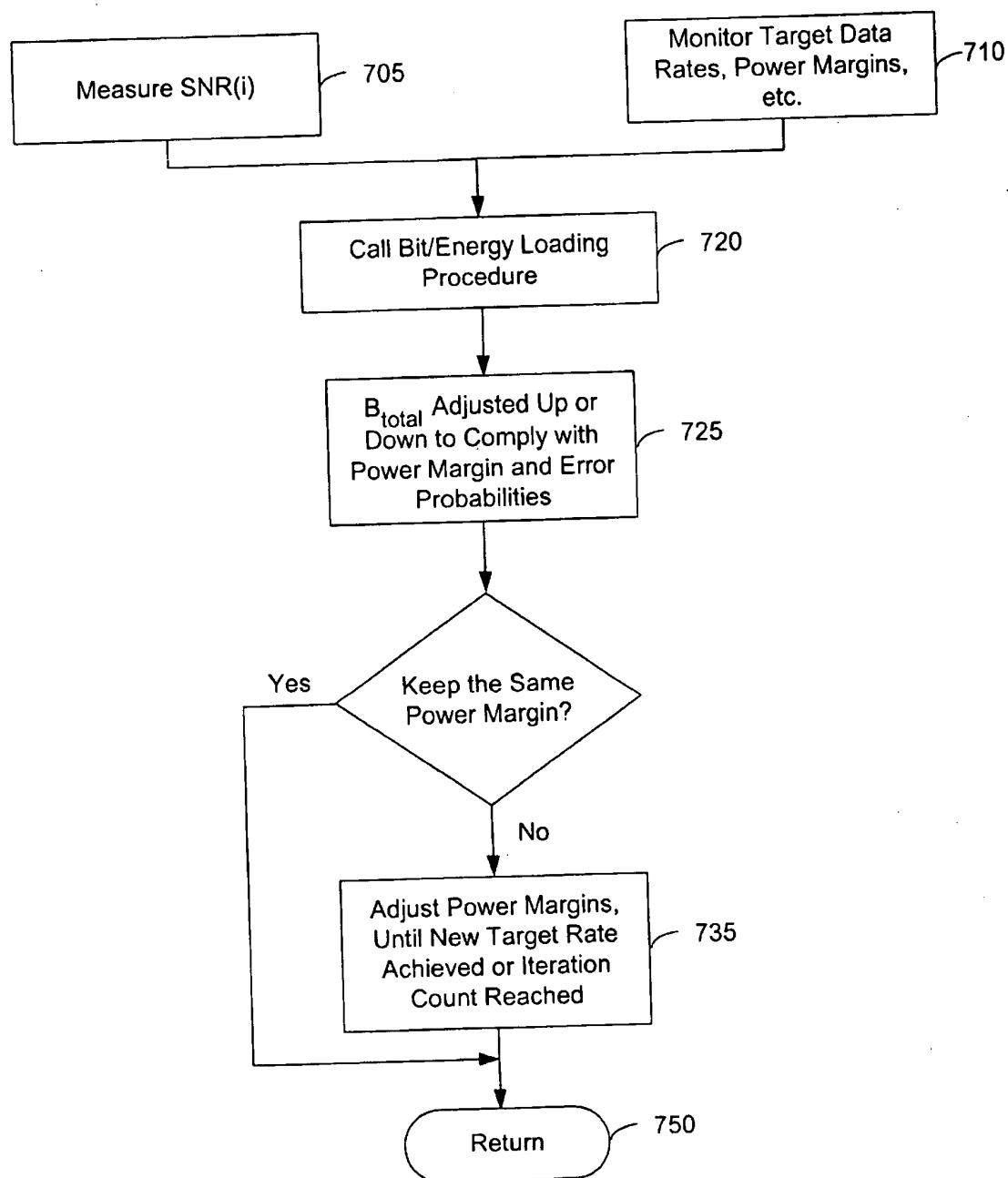


FIGURE 8

